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Multi-frequency EIT system with radially symmetric architecture: KHU Mark1

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Abstract

We describe the development of a multi-frequency electrical impedance tomography (EIT) system (KHU Mark1) with a single balanced current source and multiple voltmeters. It was primarily designed for imaging brain function with a flexible strategy for addressing electrodes and a frequency range from 10 Hz–500 kHz. The maximal number of voltmeters is 64, and all of them can simultaneously acquire and demodulate voltage signals. Each voltmeter measures a differential voltage between a pair of electrodes. All voltmeters are configured in a radially symmetric architecture in order to optimize the routing of wires and minimize cross-talk. We adopted several techniques from existing EIT systems including digital waveform generation, a Howland current generator with a generalized impedance converter (GIC), digital phase-sensitive demodulation and tri-axial cables. New features of the KHU Mark1 system include multiple GIC circuits to maximize the output impedance of the current source at multiple frequencies. The voltmeter employs contact impedance measurements, data overflow detection, spike noise rejection, automatic gain control and programmable data averaging. The KHU Mark1 system measures both in-phase and quadrature components of trans-impedances. By using a script file describing an operating mode, the system setup can be easily changed. The performance of the developed multi-frequency EIT system was evaluated in terms of a common-mode rejection ratio, signal-to-noise ratio, linearity error and reciprocity error. Time-difference and frequency-difference images of a saline phantom with a banana object are presented showing a frequency-dependent complex conductivity of the banana. Future design of a more innovative system is suggested including miniaturization and wireless techniques.

Keywords: EIT, multi-frequency, impedance imaging

1. Introduction

Electrical impedance tomography (EIT) is a medical imaging method which can visualize images of conductivity and permittivity distributions inside the human body (Webster 1990, Holder 2005). In EIT, measured boundary voltages due to multiple injection currents are used to reconstruct the images. There are numerous EIT system designs in the literature (see Boone and Holder (1996), Saulnier (2005)). These may be classified into two main types. In the first type, one active current source is used to inject current between a chosen pair of electrodes at a time and a multiplexer is used to choose the electrode pair. The second type uses multiple active current sources. Here, each current source is connected to a designated electrode and current is injected through multiple electrodes simultaneously. Ideally, the sum of currents from all active current sources must be zero all the time. Voltages from all or selected electrodes may be measured; where this is undertaken simultaneously with multiple voltmeters, these are termed 'parallel' systems. Typical examples of the first and second types are Mk3.5 (Wilson *et al* 2001) and ACT-3 (Cook *et al* 1994), respectively.

In designing a new EIT system, we have considered the factors such as (i) complexity of the system, (ii) technology available for us at present and (iii) future directions of EIT system development including miniaturization and wireless interconnections. Other functional limitations in trans-impedance measurements summarized by Seagar and Brown (1987) and Brown and Seagar (1987) have also been considered. In both types of EIT systems, we believe that improvements in hardware performance are crucial to produce better images. With this goal in mind, this paper describes a new design of a multi-frequency parallel EIT system called the KHU Mark1 intended primarily for imaging brain function (Romsauerova *et al* 2006a, 2006b, Fabrizi *et al* 2006, McEwan *et al* 2006).

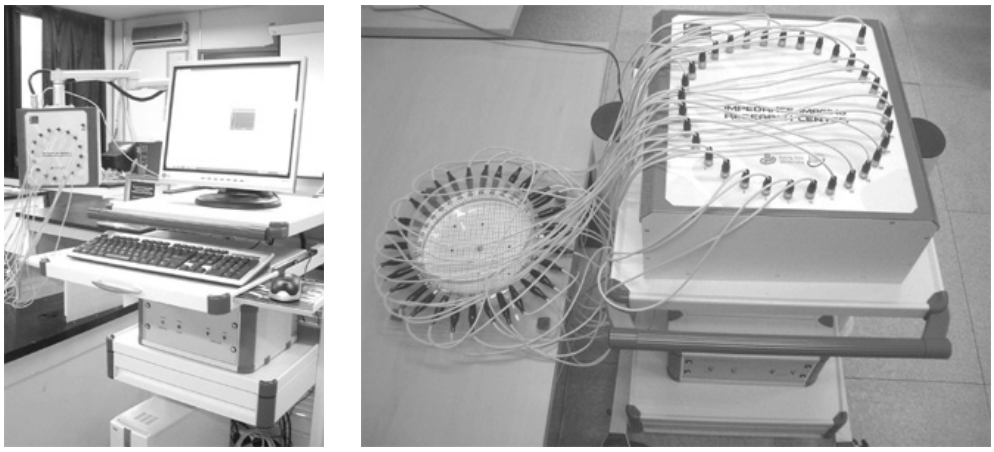
In the past, almost all successful clinical studies have employed time-difference imaging, usually at a single frequency. For imaging in acute stroke, time difference is not possible, as a single image needs to be obtained on first presentation with a stroke. One option is to attempt frequency-difference imaging, with which it is hoped that instrumentation errors might be minimized by imaging differences between frequencies. In addition, a review of literature has indicated that the largest differences across frequency occur at low frequencies below about 100 Hz. For this reason, we have designed a system which records several frequencies at once, can record down to 10 Hz and is also as accurate as possible, as the effect of the skull is to prevent passage of current into the brain, so that the resulting recorded voltage differences are small.

The KHU Mark1 EIT system belongs to the first type, having one active current source and multiple voltmeters. Even though an innovative new design of the second type has been in progress (Liu *et al* 2005, Saulnier *et al* 2006), we are not aware of any other new parallel EIT system development of the first type especially with a bandwidth of 10 Hz to 500 kHz. The purpose of this paper is to describe the design and implementation of the KHU Mark1 system. The rationale for design decisions is presented throughout. The performance of the developed EIT system was examined experimentally with resistors and saline-filled tanks.

2. Methods

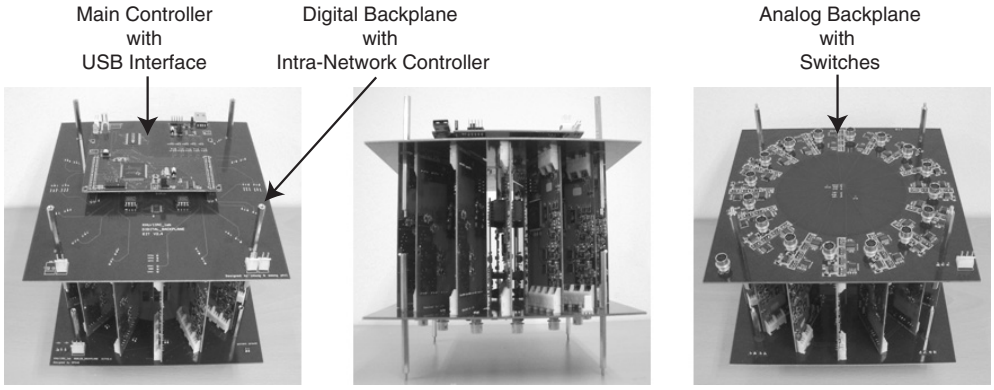
2.1. System architecture

The developed multi-frequency EIT system comprises four parts: (i) PC with USB ports and software, (ii) main body including one current source and multiple voltmeters, (iii) isolated



(a) (b)

Figure 1. Developed multi-frequency KHU Mark1 EIT system. (a) 16-channel and (b) 32-channel.



(a) (b) (c)

Figure 2. Internal views of the developed multi-frequency KHU Mark1 EIT system. (a) Top, (b) side and (c) bottom views.

dc power supply and (iv) calibrator. The main body is the core of the system; it includes a main controller, an intra-network controller on a digital backplane, a balanced current source, multiple voltmeters and switching circuits on an analog backplane. In this paper, the developed EIT system usually refers to the main body.

Figures 1(a) and (b) show the developed 16-channel and 32-channel KHU Mark1 EIT systems, respectively. Figure 2 shows the inside of the main body. The PC controls all functions of the system through the main controller shown in figure 2. The connection between them is implemented by an isolated USB interface. The main body includes a sandwich of two printed circuit boards (PCBs) with the current source and voltmeters in the middle. The current source is located at the center and voltmeters are placed around the current source in a radially symmetric way. Upper and lower PCBs holding the current source and voltmeters are the analog and digital backplane, respectively.

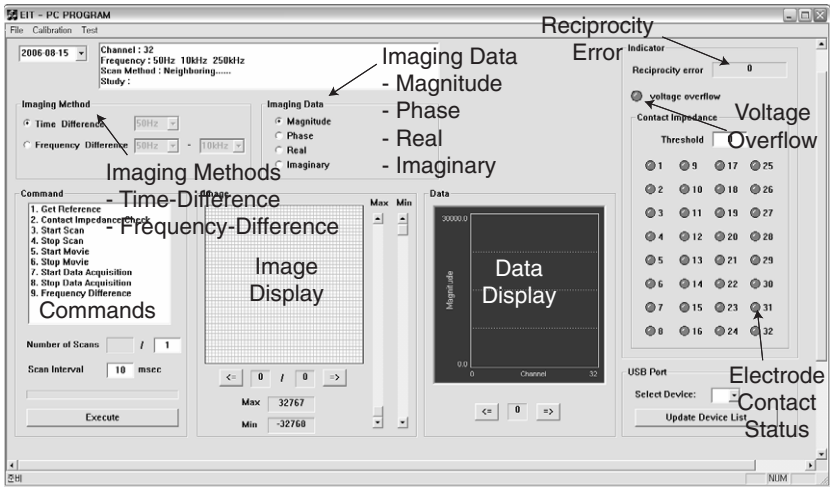


Figure 3. Developed multi-frequency EIT system software.

The data link between the main controller and all voltmeters and also the current source is called the intra-network, and it is based on multiple half-duplex high-speed serial data communication channels in a star topology. These data communication channels are arbitrated by the intra-network controller on the digital backplane. A similar approach can be found in the design of a high-speed EIT system for imaging the breast (Halter *et al* 2004). We adopted this serial intra-network to minimize the number of digital signal lines and reduce digital clock noise coupled in analog circuits.

Electrode connectors are placed along a circular path in the outer region of the analog backplane and wires are routed from the current source in the star topology. Switches on the analog backplane can choose any pair of current injection electrodes, and all electrodes have the same length of signal path from the current source.

By placing voltmeters underneath electrode connectors of the analog backplane in this radially symmetric way, all voltage measurements between neighboring pairs of electrodes are performed with almost identical signal pathways of a minimal length. In terms of a human interface, the radially symmetric architecture could be advantageous in designing an appropriate front-end for head or breast imaging. The current design described in this paper, however, excludes such a specialized front-end. Instead, it uses tri-axial cables for initial trials of a wider range of applications.

2.2. PC and software

Any PC equipped with an USB port can be used as a console of the KHU Mark1 EIT system. The PC exchanges commands and data with the main controller through the isolated USB port. Using the C-language, we developed low-level communication routines in the form of an object file or dynamic link library that can be called from other programs including Matlab (Mathworks, USA). Figure 3 shows a screen capture of the developed EIT system software running on a PC.

2.3. Main controller and PC interface

The main controller is based on a DSP (TMS320LF2407A, Texas Instruments, USA) and an USB controller (C8051F320, Silicon Laboratory, USA). The USB controller is isolated from the DSP using data isolators (ADUM1100, Analog Device, USA). Receiving commands from the PC, it controls all functions of the KHU Mark1 EIT system to collect boundary current–voltage data to be sent to the PC for image reconstructions. It provides a 40 MHz clock signal to the rest of the system for the synchronization of the current source with all voltmeters. For applications where a wireless connection to the PC is desirable, the USB controller can be interfaced to a 2.4 GHz RF serial communication module (RFW112, RFWaves, Israel). In this case, a custom-designed USB interface card including the RF module should be used at the PC side.

2.4. Intra-network controller and digital backplane

In the middle of the digital backplane in figure 2, the intra-network controller is implemented in two FPGAs (EP1K50, Altera, USA). It arbitrates commands and data between the DSP on the main controller and all voltmeters and also the current source. The intra-network controller consists of nine half-duplex synchronous serial ports with 10 Mbps data rate each. By using a time-division multiplexing scheme implemented in the FPGAs, each serial port addresses eight voltmeters. Serial communication signals and dc power lines to voltmeters are radially routed to six-pin connectors around the periphery of the digital backplane.

2.5. Current source

The balanced current source comprises two identical single-ended current sources and 12 generalized impedance converter (GIC) circuits. Six GICs are assigned to each single-ended current source. An FPGA (EP1K50, Altera, USA) in the current source contains a serial port for the intra-network connection and two digital waveform generators. For any operating frequency between 10 Hz and 500 kHz, we may inject current with a chosen single frequency at a certain moment. 16 bit data of a quarter period of the normalized sinusoid are stored in the FPGA for this kind of injection current waveform generation. Since the overall speed of the system slows down at low operating frequencies, the second waveform generator produces 16 bit waveform data of the sum of sinusoids with multiple frequencies. By default, the multiple frequency waveform is the sum of three frequencies with the relative frequency ratio of 1:5:10. Therefore, for example, currents with three low frequencies of 10, 50 and 100 Hz can be injected simultaneously. At frequencies higher than 10 kHz, we found that there is no advantage in using the multiple frequency waveform. For both waveform generators, we control the frequency or group of frequencies using an address generator inside the FPGA. The FPGA also provides a synchronization pulse marking the beginning of each or group of sinusoidal period(s). This timing pulse is broadcasted to all voltmeters through the digital backplane.

In implementing the balanced current source, passive components of the two single-ended current sources are carefully chosen so that their characteristics are as close as possible except for the polarity of their waveforms. With a 180° phase difference, one becomes the source and the other is the sink in the balanced current source. In each single-ended current source, a 16 bit DAC (AD768, Analog Devices, USA) and a first-order passive low-pass filter with 1 MHz cutoff frequency are used to convert the waveform data from the FPGA into an analog voltage signal. We can adjust the amplitude of the signal by using an 8 bit DAC (AD7801, Analog Devices, USA) that sets the reference voltage of the 16 bit DAC. The voltage signal is then

converted to current by using a voltage-to-current converter based on an improved Howland circuit (Franco 2002). The amplitude of the output current can be varied in the range of 0.2 to 2 mA peak to peak. The output of the current source is connected to a chosen pair of electrodes through a switching network using T-bar switches (MAX4545, Maxim, USA) on the analog backplane (Wilson *et al* 2001).

In order to maximize the output impedance of the current source, we used a digital potentiometer (DS1267, Dallas Semiconductors, USA) to adjust the resistance ratio of the improved Howland circuit. We found that varying phase changes occur at the output of the Howland circuit, depending on the operating frequencies. At frequencies higher than 1 kHz, these phase changes and any stray capacitance appearing at the output of the current source must be compensated to minimize the loading effect at the current source output. For this reason, we used a GIC circuit, which provides a variable inductance (Franco 2002, Ross *et al* 2003). In order to create an LC-resonance condition over the frequency range of 1 to 500 kHz, we divided the range into six subranges and assigned one GIC circuit to each subrange. For a chosen frequency belonging to a certain frequency subrange, we select the appropriate GIC circuit using CMOS switches and the fine tuning of the GIC is done using a separate digital potentiometer (DS1267, Dallas Semiconductors, USA) in the chosen GIC circuit.

2.6. Voltmeter

The voltmeter consists of the following parts: (i) shield drive circuit, (ii) differential amplifier, (iii) bandpass filter, (iv) voltage amplifier, (v) ADC and (vi) FPGA. The shield drive circuit using an operational amplifier (AD8039, Analog Devices, USA) provides both the grounded and driven shield for the tri-axial cable (SML50, Habia Cable, Sweden) (Wilson *et al* 2001). To convert a differential voltage between a pair of electrodes into a single-ended signal, we use a differential amplifier (AD8130, Analog Devices, USA) with a fixed gain of 1. The signal is then bandpass filtered to reject any dc component and high frequency noise. The filter output is connected to the voltage amplifier with a variable gain using operational amplifiers (AD8039, Analog Devices, USA). The gain is controlled by digital potentiometers (DS1267, Dallas Semiconductor, USA) with the maximal overall gain of 2500.

The cutoff frequencies of the analog bandpass filter are 10 Hz and 1 MHz. The 10 Hz low cutoff frequency is a major limiting factor in determining the overall speed of the system. We could have used switches that can change this cutoff frequency depending on the signal frequency to speed up the system at high frequencies. However, in order to prevent noise coupling at the input stage of the amplifier from switch control signals, we did not adopt this method.

The amplified signal is digitized by a 12 bit ADC (AD9235, Analog Devices, USA) at a 10 MHz sampling frequency. The digitized signal is sent to the FPGA (EP1K50, Altera, USA) where digital phase-sensitive demodulations are performed for both in-phase (real) and quadrature (imaginary) components. Since we usually use 1000 data samples for each period of a sinusoid, we adopted a non-uniform sampling technique (Cook *et al* 1994) for frequencies over 10 kHz. Digital phase-sensitive demodulation using 1000 data samples may be shown in theory to produce a signal-to-noise ratio (SNR) of 104 dB when we consider only the quantization noise (Cook *et al* 1994). However, in practice, we could seldom obtain this SNR due to other sources of noise and interference. To increase the SNR by reducing the random noise, we implemented a signal averaging method with a variable number of averages. We can average up to 64 sinusoidal periods of data but it slows down the demodulation process, so that a tradeoff between SNR and speed occurs.

The FPGA also includes a half-duplex synchronous serial port for the intra-network, a digital filter for spike noise rejection and an automatic gain controller. The spike noise rejection filter calculates a difference of two consecutive ADC data. It then replaces the latest data with the previous one if the difference exceeds a pre-determined threshold. When the automatic gain control is turned on, the FPGA first finds the average power of voltage data in one sinusoidal period. Then, it adjusts the gain of the voltage amplifier so that the computed signal power reaches 95% of the maximal average power of the sinusoid with its peak-to-peak value spanning the full scale of the ADC.

When a voltmeter is connected to a current injection electrode, it can measure the electrode contact impedance or the amount of current being injected through the electrode. When the amplitude of the voltage signal at the input of the ADC exceeds the ADC input range for a pre-determined consecutive number of samples, the voltmeter generates an overflow flag. These auxiliary information are sent to the console PC and displayed on the screen.

Since the system uses just one balanced current source, the transition times while electrode pairs are switched to the current source needed to be carefully regulated. In addition, when operating frequency changes, a wait stage in the demodulator is inserted in order to compensate for the frequency-dependent system delay. For these reasons, we designed the voltmeter in such a way that a variable amount of wait stage could be inserted before demodulation. For the operating frequency change without electrode switching, we insert two periods of the chosen sinusoidal frequency as the wait stage. When electrode switching occurs, we usually insert a 15 ms or less wait stage. We found that it is not necessary to wait until the output of the analog bandpass filter with 10 Hz low cutoff frequency settles down within, for example, 0.1%. As long as the peak-to-peak voltage signal is preserved at the input of the ADC without overflow, the phase-sensitive digital demodulation can effectively reject a slowly varying baseline drift.

2.7. Analog backplane, switching circuit and tri-axial cable

The analog backplane includes T-bar switches (MAX4545, Maxim, USA) for routing injection current to a chosen pair of electrodes and choosing two input signals of each voltmeter (figure 4). Switch S1 is used to ground the selected electrode momentarily to discharge any stored charge from a previous current injection. The injection current passes through the current-sensing resistor R_s placed in series with the current flow path, and a voltmeter can measure the current by sensing the voltage difference across the resistor instead of the usual voltage difference between a pair of electrodes. In order to connect the voltmeter either to a pair of electrodes or to two terminals of the current-sensing resistor, switches S2 and S3 are used. Switches S4 and S5 are used to inject source and sink current, respectively, to a chosen pair of electrodes. All of these switches are controlled by the FPGA in each voltmeter based on commands from the main controller.

2.8. System calibration

In view of the errors introduced by variable frequencies, electrode combinations and loads likely to be addressed, careful calibration was needed.

2.8.1. Current source calibration. To reduce the loading effect at the current source output down to, for example, 0.1%, the output impedance of the current source needed to be greater than 1 MΩ for a maximal load of 1 kΩ. Since the balanced current source consists of two single-ended current sources, we calibrated each single-ended current source separately using a current source calibration circuit. We adopted the current source calibration method described

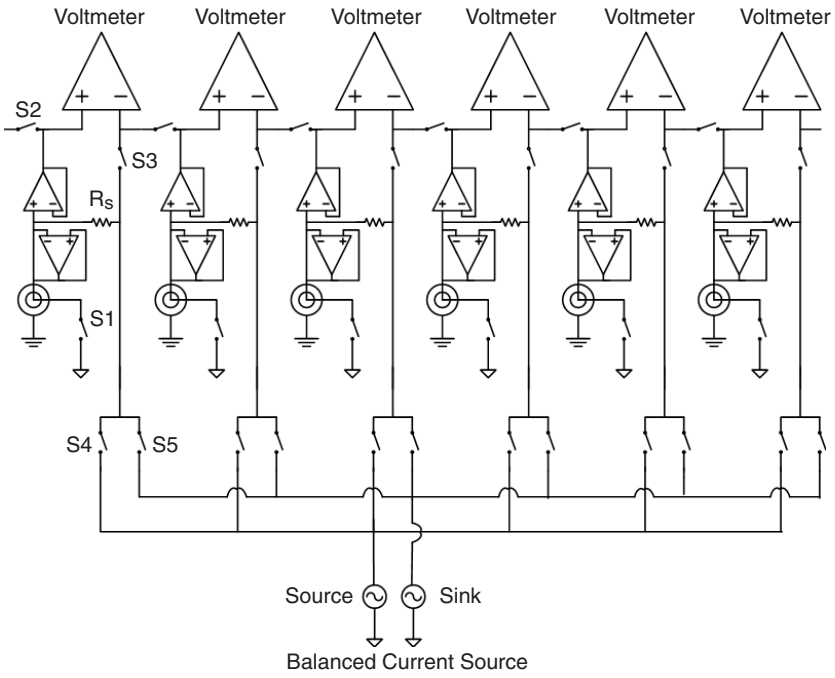


Figure 4. A portion of switching circuits on the analog backplane.

by Cook *et al* (1994) that is based on two trans-impedance measurements with and without a fixed load resistance. In our multi-frequency system, this calibration is performed for each frequency to be used. For a chosen frequency, we maximize the output resistance by using the digital potentiometer inside the Howland circuit. At any frequency higher than or equal to 1 kHz, we minimize the output capacitance by adjusting the digital potentiometer inside the selected GIC circuit. In order to maximize the output resistance and minimize the output capacitance at the same time, iterative tunings of the two potentiometers are needed since they influence each other (Ross *et al* 2003). The final potentiometer settings are stored in the PC as a current source calibration table.

2.8.2. Voltmeter calibration. A resistor phantom was used which had known resistance values through the use of a high-precision digital multi-meter (3458A, Agilent, USA). It was similar to the wheel phantom suggested by Griffiths (1995), but comprised only resistors. Voltmeter calibrations were performed in two steps of intra- and inter-channel calibrations. The intra-channel calibration calibrated each voltmeter for any possible different gains at different frequencies. 32 different gains were selected from a total 65 536 possible gains. For the choice of frequencies, 10 from 4096 possible frequencies in the range of 10 Hz–500 kHz were chosen. In this case, after the intra-channel calibration, a three-dimensional table of numbers was produced which contained $32 \times 10 \times E$ entries, where E is the number of voltmeters.

The characteristics of all voltmeters differed. In order to compensate for inter-channel variations, all voltmeters were connected to the resistor phantom and measured a full set of voltage data for a chosen set of injection currents. The amplitude and phase of the measured voltage data were compared to the numerically computed ideal values. This produced a scaling

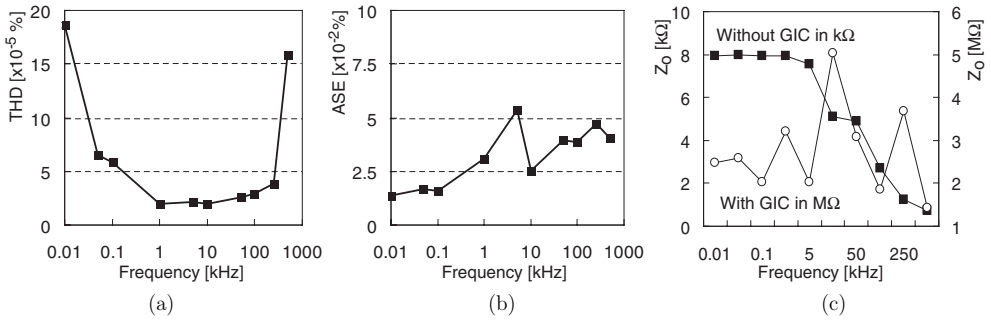


Figure 5. (a) Total harmonic distortion (THD), (b) stability error (SE) and (c) output impedance of the current source over the frequency range.

factor of a complex number for each voltage datum in the full data set. The inter-channel calibration table including all of these complex numbers was also stored in the PC. Performing both intra- and inter-channel calibration takes several hours since our system operates at frequencies as low as 10 Hz.

2.9. Experimental performance evaluation

For the current source, we measured the total harmonic distortion (THD), amplitude stability error (ASE) and output impedance (Z_o). To verify the performance of voltmeters, we measured the common-mode rejection ratio (CMRR), SNR, reciprocity error (RE) and linearity error (LE). For RE and SNR measurements, we used a two-dimensional homogeneous saline phantom with 200 mm diameter, 100 mm height and 0.137 S m^{-1} conductivity. For imaging experiments, we placed a banana (30 mm diameter and 50 mm length) inside the saline phantom with a background conductivity of 0.05 S m^{-1} and collected a full set of data at the chosen frequencies from 10 Hz to 500 kHz. Time- and frequency-difference images were produced using a difference image reconstruction algorithm based on the sensitivity matrix (Mueller *et al* 1999, Lionheart *et al* 2005).

3. Results

3.1. Basic performance tests

3.1.1. Current source. To test the developed KHU Mark1 EIT system over the frequency range of 10 Hz to 500 kHz, we chose ten frequencies of 10, 50, 100, 1000, 5000, 10 000, 50 000, 100 000, 250 000 and 500 000 Hz. The THD of the current source waveforms at these frequencies were less than 0.0002% (figure 5(a)). Collecting N periods of sinusoidal waveform data over 1 h, we defined the ASE as

$$\text{ASE} = \frac{\text{standard deviation}(p_1, p_2, \ldots, p_N)}{\text{mean}(p_1, p_2, \ldots, p_N)} \times 100\%,$$

where p_i with $i = 1, \ldots, N$ is the signal power of one period of the ith sinusoidal waveform. The ASEs were less than 0.06% at the chosen frequencies over 1 h (figure 5(b)). For a short time period, we found that the ASE was negligibly small.

Without matching resistance values in the Howland circuit and also without using GIC circuits, the output impedance was about 8 kΩ and rapidly decreased beyond 1 kHz

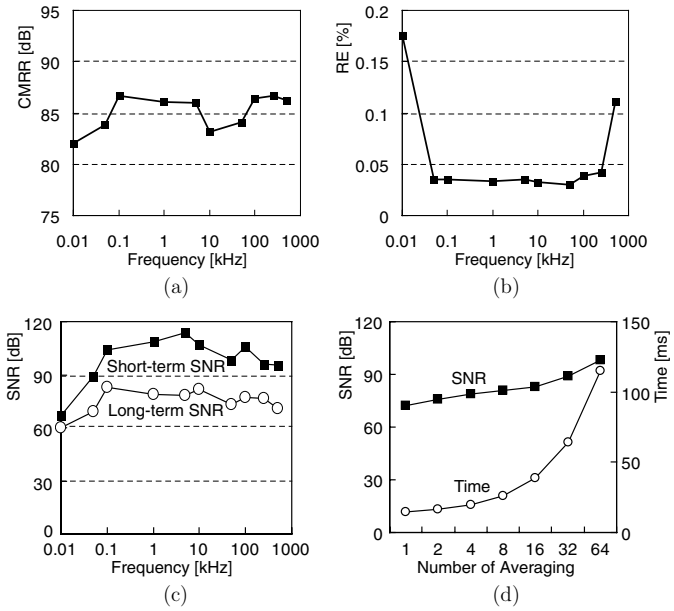


Figure 6. Voltmeter performances: (a) CMRR, (b) RE and (c) SNR over the frequency range. (d) SNR at 50 kHz improves as we increase the number of averages. We have to slow down the voltage measurement process to achieve a higher SNR.

(figure 5(c)). By a careful matching of resistance values and with the use of GIC circuits, the output impedance increased to greater than 1 MΩ for the chosen frequencies. Since we used the developed voltmeter to measure the output impedance of the current source, the voltmeter SNR described later should have affected the results.

3.1.2. Voltmeters. CMRR was recorded with a 100 Ω series resistor inserted at one input. It was around 85 dB for all frequencies (figure 6(a)). Using the homogeneous saline phantom with 0.137 S m^{-1} conductivity, RE was around 0.05% from 50 Hz to 250 kHz. At the lowest and highest frequencies of 10 Hz and 500 kHz, RE was 0.17 and 0.11%, respectively (figure 6(b)). Without proper calibration, RE could be as much as 5%. Short-term (1 h) and long-term (2 days) SNRs were defined as the ratio of mean to standard deviation of 100 measurements from the homogeneous saline phantom. By using the maximal number (64) of data averages, average short- and long-term SNRs were 99 and 76 dB, respectively (figure 6(c)). The smaller long-term SNR indicates that the system characteristics drift over days mainly due to changes in temperature and power supply voltage. With fewer averages, the SNR was lower for shorter data acquisition times (figure 6(d)). When the number of averages was bigger than 16, the improvement in SNR was greater than the theoretically expected value. We speculate that the randomness of jittering of the synchronization pulse used in the demodulator increases as we increase the number of averages. The time for the demodulation in figure 6(d) is not perfectly proportional to the number of averages since there exists a fixed amount of common setup time in the demodulation process.

In order to verify the linearity of voltage measurements, five pairs of resistors (R_1, R_2) were used. Their resistance values were directly measured with a high-precision digital multi-meter (3458A, Agilent, USA). We simulated skin impedances as shown in figure 7(a)

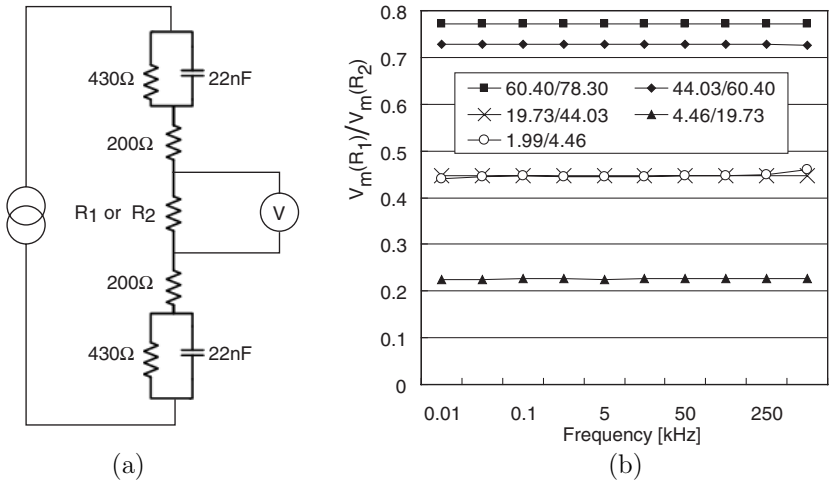


Figure 7. (a) Setup for the linearity test using simulated skin impedances. (b) Plots of ratios of measured voltages across two resistors. For example, 60.40/78.30 means that we chose two resistors of $R_1 = 60.40$ and $R_2 = 78.30\ \Omega$ with the ratio of 0.77.

and placed the chosen resistor R_1 or R_2 at the middle of them. Current was applied through the simulated skin impedances, and voltage was recorded across the resistor at all chosen frequencies. Figure 7(b) shows plots of $V_m(R_1)/V_m(R_2)$ for the chosen frequencies where $V_m(R_1)$ and $V_m(R_2)$ are measured voltages using R_1 and R_2, respectively. Ideally, each plot of $V_m(R_1)/V_m(R_2)$ should be flat over the frequency range with one value that is equal to R_1/R_2. LE was therefore defined as

$$\mathrm{LE} = \max \left| \frac{R_1}{R_2} - \frac{V_m(R_1)}{V_m(R_2)} \right| \times 100\%.$$

From the plots in figure 7(b), we found that the LE is between 0.11 and 0.16%.

3.2. Saline phantom imaging tests

We collected the first set of multi-frequency data from the homogeneous saline phantom with 0.05 S m^{-1} conductivity. Placing the banana (30 mm diameter and 50 mm length) inside the phantom, we collected the second set of multi-frequency data. Using both data sets with the first one as the reference data, we reconstructed time-difference images at multiple frequencies (figure 8(a)). Frequency-difference images were reconstructed using the second data set with the data at 100 Hz as the reference (figure 8(b)). For both time- and frequency-difference image reconstructions, we separately produced real and imaginary part images using real and imaginary parts of the voltage data, respectively.

In figure 8(a), we can see that the complex conductivity of the banana changes with frequency. We measured the conductivity of the banana using the impedance analyzer (4192A, Agilent Technologies, USA), and it increased from 0.01 S m^{-1} at 10 Hz to 0.17 S m^{-1} at 500 kHz. Interestingly, the real part image at 50 kHz does not show the banana and its contrast with respect to the background of 0.05 S m^{-1} is reversed in the images at 100 and 250 kHz. As expected, at low frequencies of 50 and 100 Hz, the imaginary part images do not show the banana object clearly. The frequency-difference images in figure 8(b) show that the banana object is distinguished at frequencies over 1 kHz when the reference data are at 100 Hz.

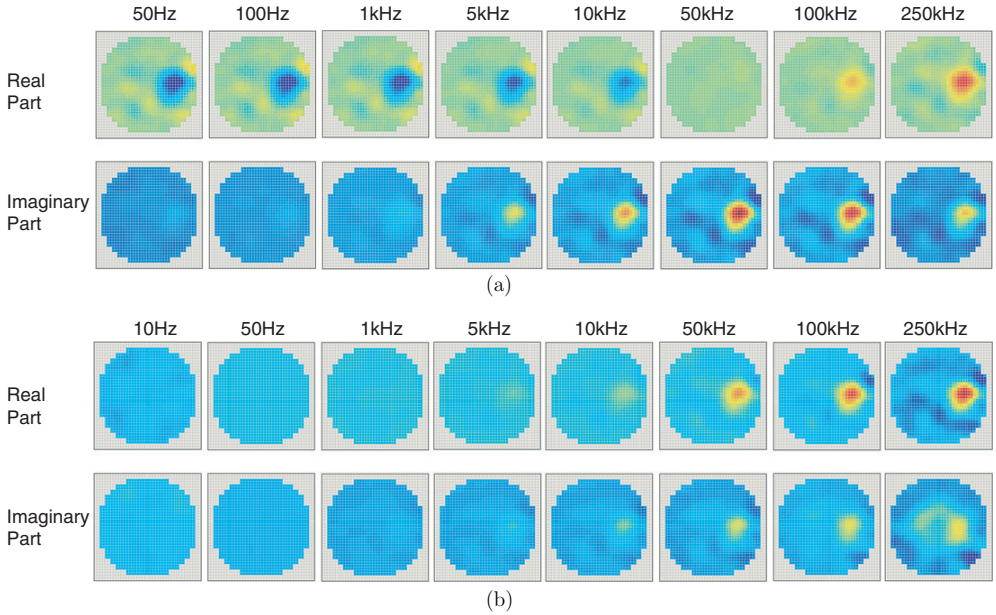


Figure 8. (a) Time-difference images of a banana object inside the saline phantom. Reference data were obtained from the homogeneous phantom at each frequency. (b) Frequency-difference images of the same banana object with the data at 100 Hz as the reference data. All images at the same row are displayed with the same scale.

(This figure is in colour only in the electronic version)

A more thorough quantitative image analysis will be included in our future works on numerous imaging experiments.

4. Discussion and conclusion

The radially symmetric structure of the KHU Mark1 EIT system is advantageous in terms of SNRs and reciprocity errors. The intra-network with the star topology turned out to be effective for reduction of digital clock noise in the analog circuits. Separation of digital and analog backplane was also very helpful. We found that T-bar switches and tri-axial cables are advantageous due to their very low cross-talk and stray capacitances (Wilson *et al* 2001). In using the driven shield of the tri-axial cable, a series resistor should be inserted inside the cable to prevent high frequency oscillation. The two-step calibrations of intra- and inter-channel calibrations were essential in preserving the high performance of the system especially in terms of the reciprocity error.

In choosing the bandwidth of the KHU Mark1 EIT system, we considered the following. First, the lowest frequency of 10 Hz was decided based on its need for the brain imaging (Yerworth *et al* 2002, 2003). The highest frequency of 500 kHz was determined based solely on measured performance. Even though measurements at frequencies higher than 1 MHz could be valuable in applications such as breast imaging (Halter *et al* 2004) or hemorrhage in the brain, we found that, in our system, the measurement errors significantly increased beyond 500 kHz.

We had to compromise some performance in order to implement the multi-frequency capability. We used wide-band amplifiers from 10 Hz to 1 MHz, and these are more vulnerable

to external noise. In order to maximize the output impedance of the current source from 10 Hz to 500 kHz, we had to use multiple GICs and change the setting of a chosen GIC using the stored current source calibration table. At low frequencies, phase-sensitive demodulations in voltmeters take a longer time due to long sinusoidal periods. Consequently, the data acquisition time is increased and slowed down the entire system. Using eight frequencies, we found that the maximum frame rate of the 32-channel system was about 3 frames s^{-1}. Since it depends on many factors including the number of averages and chosen frequencies as well as the image reconstruction algorithm, it will be possible to improve the temporal resolution by optimizing both hardware and software in the future.

The developed KHU Mark1 EIT system will be thoroughly tested with a few clinical applications in mind. We will perform numerous time- and frequency-difference imaging experiments with a quantitative image analysis. We hope it finds clinical usefulness in application areas including stroke-type detection, monitoring of stomach emptying, pulmonary monitoring and others. For the future, we plan miniaturization and wireless interconnections. As in other EIT systems, we found that bulky cables and dc power supplies are cumbersome. For certain applications, it will be very useful to miniaturize the system, possibly with small batteries as power sources.

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