

CASPEN Visitor program exit report

The PUEO experiment, held its annual collaboration meeting in June. The collaboration mainly centres out of American Midwest Universities and Hawaii. UCL is one of two non-American University involved and the only European organisation. PUEO's UCL size is also limited.

Due to time zone challenges and a little in person cooperation it had been a challenge to ingratiate myself within the collaboration.

I had recently been working through testing how the FPGA ZCU-111 handles inputs. This was somewhat unstructured without clear goals and mainly consisted of my developing the collaborations python DAQ (Data Acquisition) program.

It seemed very beneficial to utilise that I would already be at OSU (host of meeting) to stay for a total of 2 weeks. I was hoping to work more with Patrick Allison at OSU and other members of hardware/firmware team. Particularly to see their lab testing setup, have more structured work assignments and also to see how people were using the amended DAQ program.

I had hoped to do something similar with the simulations and analysis team but a lot of people attended ARENA conference and as it happened I was too busy in the lab.

The time in the OSU lab was incredibly informative. The lab was huge and using the hardware around the FPGA has informed me of further methods of testing the FPGA with equipment we have at UCL. OSU's setup on the board itself is somewhat archaic and the ZCU111 was not connected to a lab network (or internet) leading to difficulties cloning my DAQ program. Combined with its specific setup meant it hadn't been used at OSU. I had not realised it needed to be amended.

After completely restructuring the entire program to make it out the box runnable I also created base programs for one to simply write testing code in a testing space, which is both in general easier to use but a lot easier to write testing code on the FPGA itself.

Patrick set me to work testing the AGC (Automatic Gain Control) component of PUEO's FPGA firmware. Me and, fellow OSU PhD student, Taylor went through testing the AGC and now it is fully operational.

The AGC itself does 12- to 5-bit conversion. Example of things to be tested included the firmware's accumulator, which effectively uses significantly less data to calculate the RMS of any input waveform and the PID controller responsible for maintaining a input at constant amplitude.

My time collaborating with people in lab has given me further confidence to take back to UCL's lab and I now have a better idea of how my time would best be spent. The AGC's performance still needs to be accurately benchmarked and the biquad filter firmware needs

to be tested from scratch. Other tasks could include getting the ZCU's RPU to run effectively and replay previous experimental data acquisitions through the new hardware and firmware.

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