Performance Portability across Diverse Computer Architectures
Recent processor trends in HPC

Many-core CPUs

GPU/accelerators

FPGAs

http://uob-hpc.github.io
AMD’s Rome showing where mainstream CPUs are heading

From late 2019:

• Up to 64 heavyweight x86 cores per CPU
• Uses 8 chiplets of 8 cores each, plus an I/O chiplet

Chiplets likely to be an important future trend...

http://uob-hpc.github.io
Emerging competition from Arm CPU vendors

CAVIUM

FUJITSU

AMPERE

http://uob-hpc.github.io
An example forthcoming Arm-based CPU: Fujitsu’s A64FX

• 48 cores, no hyperthreading
• 2.7 TFLOP/s double precision, 512-bit vectors (SVE)
• 1 TeraByte/s main memory bandwidth
  • 32 GB HBM2
• ~170 Watts
• High speed interconnect
• 8.7B transistors, 7nm
• Fugaku now installed at RIKEN
  • 158,976 A64FX processors

NEC Aurora Vector Engine sit at technology intersection

• Relatively few cores (8) compared to CPUs (64) and GPUs (80)
  • More cores increase FLOPs, but also increase aggregate cache size and bandwidth
• Hierarchy of large caches like a CPU
• Wide vectors like a GPU (32 VPU's / 256 FP64 vectors)
• Uses HBM2 memory technology
• Accelerator form-factor, but traditional programming model
  • Reverse offload MPI+OpenMP
  • Standard offload an option too

http://uob-hpc.github.io
Recent architectural trends

• CPUs have evolved to include lots of cores and wide vector units

• 32 core CPUs now common (AMD Naples, Marvell ThunderX2)

• 48, 64 core CPUs arrive within the next 12 months (A64fx, Rome)

• Chiplet manufacturing processes likely to be an important future trend

• This renewed competition in CPUs is crucial to the health of the HPC ecosystem, and for performance per dollar

• GPUs incorporating latest memory technologies (HBM)
  • So do KNL and A64FX CPUs

• GPUs have lots of cores and very wide vector units

• Lightweight cores becoming more complex (caches, specialised accelerators, etc)

• Vendor competition increasing (AMD GPUs in Frontier, Intel GPUs in Aurora, NVIDIA GPUs pre-Exascale Perlmutter)
Isambard system specification

• **10,752** Armv8 cores (168n x 2s x 32c)
  • Marvell ThunderX2 32 core 2.1→2.5GHz
  • 256 GB RAM per node, bandwidth >240 GB/s
• Cray XC50 ‘Scout’ form factor
• High-speed **Aries** interconnect
• Cray HPC optimised software stack
  • CCE, Cray MPI, math libraries, CrayPAT, ...

• **Phase 2 (the Arm part):**
  • Installed in November 2018, accepted in 1 week!
  • Upgraded silicon (to B2), firmware and stack Mar19
  • As of June (since increased):
    185 registered users, 63 are external
  • **PRODUCTION SERVICE** opened to all users May 2019
    • First Arm-based production service in the world!

http://gw4.ac.uk/isambard/
Comparing between multiple Arm-based supercomputers

- **Bristol** is one of the few sites in the world with multiple different Arm-based supercomputers
  - Added an HPE Catalyst system in 1Q2019
    - 64-node Apollo70 system, 4,096 cores, ThunderX2 CPUs

- **Isambard** and **Catalyst** together enable us to compare across:
  - **Networks**: Cray Aries vs Mellanox IB
  - **Software stacks**: open source vs Cray

• For comparisons see following references:
  • Talk from AHUG @ISC’19
  • [https://doi.org/10.1002/cpe.5110](https://doi.org/10.1002/cpe.5110)
  • [http://gw4.ac.uk/isambard/](http://gw4.ac.uk/isambard/)
GROMACS (42 million atoms, ARCHER benchmark)

Scaling Results From the First Generation of Arm-based Supercomputers
S. McIntosh-Smith, J. Price, A. Poenaru and T. Deakin, CUG 2019, Montreal
Isambard 2 Tier-2 service designed to explore these opportunities

Diverse range of architectures:

- **CPUs:**
  - Arm: Fujitsu, Marvell
  - X86: AMD, Intel
  - IBM POWER

- **GPUs:**
  - NVIDIA
  - AMD
  - Intel

http://uob-hpc.github.io
Challenges at Exascale

- The coming generation of Exascale supercomputers will contain a diverse range of architectures at massive scale

  - **Perlmutter**: AMD EYPC CPUs and NVIDIA GPUs (pre-Exascale)
  - **Frontier**: AMD EPYC CPUs and Radeon GPUs
  - **Aurora**: Intel Xeon CPUs and Xe GPUs
  - **El Capitan**: AMD EPYC CPUs and Radeon GPUs
  - **Fugaku**: Fujitsu A64fx Arm CPUs

The Next Platform, Jan 13th 2020: “HPC in 2020: compute engine diversity gets real”
High performance in silico virtual drug screening on many-core processors

Simon McIntosh-Smith, James Price, Richard B Sessions

On the Performance Portability of Structured Grid Codes on Many-Core Computer Architectures

Simon McIntosh-Smith, Michael Baillot, Don Curran, and James Price

Assessing the performance portability of modern parallel programming models using Tealleaf

Matthew Martinez, Simon McIntosh-Smith, Wayne Gaudin

Evaluating attainable memory bandwidth of parallel programming models via BabelStream

Tom Deakin*, James Price, Matt Martinez, and Simon McIntosh-Smith

Department of Computer Science, University of Bristol, Bristol, UK
Email: t.deakin@bristol.ac.uk
Email: m.martinez@bristol.ac.uk
Email: s.mcintosh@bristol.ac.uk
*Corresponding author

Department of Computer Science, University of Bristol, Bristol, UK

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WILEY

http://uob-hpc.github.io/publications/
What do we mean by “performance portability?”

“A code is performance portable if it can achieve a similar fraction of peak hardware performance on a range of different target architectures.”

Questions:

• Does it have to be a “good” fraction? YES! Within 20% of “best achievable”, i.e. of hand-optimized OpenMP, CUDA, ...

• How wide is the range of target architectures? Depends on your goal, but important to allow for future architectural developments
A Metric for Performance Portability

S. J. Pennycook, J. D. Sewall and V. W. Lee
Intel Corporation
Santa Clara, California
{john.pennycook.jason.sewall.victor.w.lee}@intel.com

Abstract — The term “performance portability” has been informally used in computing to refer to a variety of notions which generally include: 1) the ability to run one application across multiple hardware platforms; and 2) achieving some notional level of performance on these platforms. However, there has been a noticeable lack of consensus on the precise meaning of the term, and authors’ conclusions regarding their success (or failure) to achieve performance portability have thus been subjective. Comparing one approach to performance portability with another has generally been marked with vague claims and verbose, qualitative explanation of the comparison. This paper presents a concise definition for performance portability, along with a simple metric that accurately captures the performance and portability of an application across different platforms. The utility of this metric is then demonstrated with a retroactive application to previous work.

and demonstrate its accuracy and utility for quantifying an application’s performance and portability; and
3) We retroactively apply our metric to a number of published application studies, thereby highlighting the utility of a shared metric when comparing and contrasting different approaches to performance portability.

II. RELATED WORK

There have been a number of efforts to develop new programming models, languages and tools that provide users with a productive means of achieving performance portability. Some have proposed the use of domain-specific languages (DSLs), providing a limited set of high-level abstractions for a spe-
Two ways to measure Performance Portability

Definitions from the Pennycook, Sewall and Lee paper:

1. **Architectural efficiency:**
   Achieved performance as a *fraction of peak theoretical hardware performance*. This represents the ability of an application to utilize hardware efficiently;

2. **Application efficiency:**
   Achieved performance as a *fraction of best observed performance*. This represents the ability of an application to use the most appropriate implementation and algorithm for each platform.
A systematic evaluation of Performance Portability

• Studying Performance Portability is hard!
  • Have to be rigorous about doing as well as possible across a wide range issues: architectures, programming languages, algorithms, compilers, ...

• It takes a lot of effort to do this well

• Motivated by our results so far, in Bristol we have initiated a wide-ranging evaluation of Performance Portability:
  • Across many codes
  • Across many programming languages
  • Across many architectures

• Our goal is to share these codes and results to further the fundamental understanding of performance portability

http://uob-hpc.github.io
Codes in the Bristol Performance Portability study

BabelStream: simple measure of achievable memory bandwidth
CloverLeaf: structured grid hydrodynamics
TeaLeaf: structured grid heat diffusion
Neutral: Monte Carlo neutral particle transport
MiniFMM: fast multipole method
SNAP*: structured grid deterministic neutral particle transport
unSNAP*: unstructured grid deterministic neutral particle transport
MG-CFD*: unstructured grid CFD
Mini-PRECISE: combustion code

* = work in progress

http://uob-hpc.github.io
Parallel programming languages in the Bristol PP study

- OpenMP
- OpenMP target
- Kokkos CPU
- Kokkos GPU
- OpenACC

- CUDA
- OpenCL
- RAJA*
- SYCL*
- Flat MPI*

* = to come
Target hardware platforms

**CPUs:**
- Intel Skylake
- Intel KNL
- AMD Naples, Rome*
- IBM POWER9
- Marvell ThunderX2
- Marvell ThunderX3/4/5*
- Ampere eMAG
- Fujitsu A64fx*

**Accelerators:**
- NEC Aurora
- NVIDIA Turing
- NVIDIA Volta
- NVIDIA Pascal
- NVIDIA Kepler
- AMD Radeon VII
- FPGAs*

* = to come
Peak D.P. FLOP/s

Skylake: 3.76
KNL: 2.66
Power 9: 1.02
Naples: 1.02
ThunderX2: 1.28
Ampere: 0.21
NEC Aurora: 2.15
K20: 1.18
P100: 4.04
V100: 7.01
Turing: 0.37
Radeon VII: 3.50

Peak BW GB/s

Skylake: 256
KNL: 490
Power 9: 340
Naples: 288
ThunderX2: 288
Ampere: 159
NEC Aurora: 1,200
K20: 208
P100: 732
V100: 900
Turing: 616
Radeon VII: 1,024

http://uob-hpc.github.io
Bristol Performance Portability study

Latest results

http://uob-hpc.github.io
BabelStream

- BabelStream benchmark written to measure achievable (main) memory bandwidth
- Based on McCalpin STREAM benchmark, but with a number of key differences:
  - Arrays allocated on the heap
  - Problem size known only at runtime
  - Range of programming models to widen support for CPUs and GPUs
- Constructed of simple vector operations:
  - \( c[i] = a[i] \)
  - \( b[i] = \text{scalar} \times c[i] \)
  - \( c[i] = a[i] + b[i] \)
  - \( a[i] = b[i] + \text{scalar} \times c[i] \)
  - \( \text{sum} += a[i] \times b[i] \)

https://github.com/UoB-HPC/BabelStream
## Achieved bandwidth (GB/s)

<table>
<thead>
<tr>
<th></th>
<th>OpenMP</th>
<th>Kokkos</th>
<th>CUDA</th>
<th>OpenACC</th>
<th>OpenCL</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Skylake</strong></td>
<td>205</td>
<td>174</td>
<td>-</td>
<td>83.0</td>
<td>107</td>
</tr>
<tr>
<td><strong>KNL</strong></td>
<td>452</td>
<td>304</td>
<td>-</td>
<td>444</td>
<td>286</td>
</tr>
<tr>
<td><strong>Power 9</strong></td>
<td>248</td>
<td>250</td>
<td>-</td>
<td>247</td>
<td>-</td>
</tr>
<tr>
<td><strong>Naples</strong></td>
<td>190</td>
<td>181</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>ThunderX2</strong></td>
<td>246</td>
<td>244</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Ampere</strong></td>
<td>106</td>
<td>91.1</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>NEC Aurora</strong></td>
<td>976</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>K20</strong></td>
<td>144</td>
<td>152</td>
<td>150</td>
<td>-</td>
<td>151</td>
</tr>
<tr>
<td><strong>P100</strong></td>
<td>553</td>
<td>557</td>
<td>552</td>
<td>552</td>
<td>551</td>
</tr>
<tr>
<td><strong>V100</strong></td>
<td>774</td>
<td>828</td>
<td>833</td>
<td>829</td>
<td>839</td>
</tr>
<tr>
<td><strong>Turing</strong></td>
<td>528</td>
<td>554</td>
<td>556</td>
<td>555</td>
<td>554</td>
</tr>
<tr>
<td><strong>Radeon VII</strong></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>814</td>
</tr>
</tbody>
</table>

## Architectural efficiency (Fraction of hardware peak)

<table>
<thead>
<tr>
<th></th>
<th>OpenMP</th>
<th>Kokkos</th>
<th>CUDA</th>
<th>OpenACC</th>
<th>OpenCL</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Skylake</strong></td>
<td>80.2%</td>
<td>68.1%</td>
<td>-</td>
<td>32.4%</td>
<td>41.8%</td>
</tr>
<tr>
<td><strong>KNL</strong></td>
<td>92.2%</td>
<td>62.1%</td>
<td>-</td>
<td>90.7%</td>
<td>58.4%</td>
</tr>
<tr>
<td><strong>Power 9</strong></td>
<td>72.8%</td>
<td>73.6%</td>
<td>-</td>
<td>72.5%</td>
<td>-</td>
</tr>
<tr>
<td><strong>Naples</strong></td>
<td>65.9%</td>
<td>62.7%</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>ThunderX2</strong></td>
<td>85.3%</td>
<td>84.7%</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Ampere</strong></td>
<td>66.4%</td>
<td>57.3%</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>NEC Aurora</strong></td>
<td>81.3%</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>K20</strong></td>
<td>69.2%</td>
<td>72.9%</td>
<td>72.3%</td>
<td>-</td>
<td>72.8%</td>
</tr>
<tr>
<td><strong>P100</strong></td>
<td>75.5%</td>
<td>76.1%</td>
<td>75.4%</td>
<td>75.3%</td>
<td>75.3%</td>
</tr>
<tr>
<td><strong>V100</strong></td>
<td>86.0%</td>
<td>92.0%</td>
<td>92.6%</td>
<td>92.1%</td>
<td>93.2%</td>
</tr>
<tr>
<td><strong>Turing</strong></td>
<td>85.7%</td>
<td>90.0%</td>
<td>90.2%</td>
<td>90.1%</td>
<td>89.9%</td>
</tr>
<tr>
<td><strong>Radeon VII</strong></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>79.4%</td>
</tr>
</tbody>
</table>
Performance portability

• Heatmaps can give an intuitive view on performance portability
  • Want to be rigorous, so use the Performance Portability metric to quantify the intuition

• The challenge is that no language runs successfully on all our platforms.

• We automatically create platform subsets and compute performance portability of application efficiency for each subset
  • Start with all platforms (PP = 0)
  • Remove the platform which is the least supported (the one with the most missing results)
  • If tied, remove the platform which causes biggest change in L₂-norm of performance portability from current platform subset

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Observations on BabelStream Performance Portability

- If we exclude the AMD Radeon GPU, then **OpenMP** successfully runs on all the remaining platforms, with PP = 97.5%
- Excluding the NEC Aurora, then **Kokkos** can run across the remaining set with PP = 89.3%
- If we further exclude all non-Intel CPUs, then **OpenCL** runs with PP = 76.7% ($|H|=8$)
  - Improves if only consider GPUs due to NUMA related runtime issues
- Also excluding Power 9, AMD Naples and NVIDIA K20, **OpenACC** will run with similar portability to **OpenCL**.
  - Do have Power 9 result, but heuristic chose to keep K20 where we don’t

http://uob-hpc.github.io
Performance Portability of OpenMP and Kokkos

- Heatmap shows PP metric on chosen platform subsets
- Rows indicate how a model fairs across different applications
- OpenMP achieving best performance on CPUs but struggles on GPUs due to support
- Kokkos shows a small overhead on CPUs
  - PP metric tells us to expect the abstraction of OpenMP/CUDA to reduce performance by ~15-50%

- Final row here (Kokkos all) shows performance portability is possible
  - Mean and standard deviation shows we would expect Kokkos to achieve 59-79% of best application performance on average

<table>
<thead>
<tr>
<th></th>
<th>BabelStream</th>
<th>TeaLeaf</th>
<th>CloverLeaf</th>
<th>Neutral</th>
<th>MiniFMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>OpenMP CPU</td>
<td>98.4%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
</tr>
<tr>
<td>Kokkos CPU</td>
<td>83.0%</td>
<td>49.8%</td>
<td>60.7%</td>
<td>77.6%</td>
<td>66.1%</td>
</tr>
<tr>
<td>OpenMP GPU</td>
<td>95.5%</td>
<td>22.5%</td>
<td>0.0%</td>
<td>0.0%</td>
<td>0.0%</td>
</tr>
<tr>
<td>Kokkos GPU</td>
<td>99.5%</td>
<td>64.3%</td>
<td>85.7%</td>
<td>51.1%</td>
<td>60.4%</td>
</tr>
<tr>
<td>OpenMP all</td>
<td>97.3%</td>
<td>43.6%</td>
<td>0.0%</td>
<td>0.0%</td>
<td>0.0%</td>
</tr>
<tr>
<td>Kokkos all</td>
<td>88.5%</td>
<td>54.4%</td>
<td>68.2%</td>
<td>65.0%</td>
<td>63.9%</td>
</tr>
</tbody>
</table>

Higher is better

Mean | Std. Dev.
--- | ---
99.7 | 0.6
67.5 | 11.9
23.6 | 37.0
72.2 | 17.7
28.2 | 38.5
68.0 | 11.2

http://uob-hpc.github.io
Overall Performance Portability observations thus far

• Performance portability can be a very mixed bag
  • A language may do well on one code, then poorly on the next
• OpenMP and Kokkos achieving the best platform coverage
• Big differences between compilers for PP (esp. OpenMP target)
• Kokkos doing the best in allowing applications to achieve performance portability across architectures
  • Our PP goal was to achieve 20% of best performance, and Kokkos achieves within 32% of best performance on average
• OpenACC struggling for coverage on the CPUs (x86. A64fx? TX4?)
  • Symptom of vendor controlled, non-open/standardised programming models?
  • Hard to talk about performance portability when portability is limited
Where next for the Bristol Performance Portability study?

- Eventually aiming for about 10 codes in 8 languages across 14 platforms (980 combinations!)
- Can we achieve performance portability between CPUs and GPUs using widely supported (by vendors) industry standards?
- If not, what’s stopping us, and what can we do about it?
- Can we find good examples of codes that work well, and codes that are inherently hostile to performance portability?
- Want to push improvements in compilers, run-times, libraries, and even architectures, to improve prospects for PP
Thoughts on productivity

- Lines of code of each mini-app/model shows expected trends in verbosity of some models
- Original CloverLeaf and TeaLeaf are rather long compared to the other ports
  - Is programmer style a factor here?
- More sophisticated productivity metrics require capturing information during development
  - Hard to quantify for existing codes/ports
- Porting these mini-apps to each programming model took around 2 weeks
  - Lines of Code doesn’t amortize away developer time saved once the first parallel loop is written

---

**LOC normalised to smallest**

- BabelStream
- TeaLeaf
- CloverLeaf
- Neutral
- MiniFMM

**Measurement**

- OpenMP
- OpenMP Target
- Kokkos CPU
- Kokkos GPU
- OpenACC
- CUDA
- OpenCL

---

**Fig. 12. Normalised lines of code for each implementation of each mini-app**

http://uob-hpc.github.io
Performance Portability of SYCL

- SYCL is a single-source C++ parallel programming model for heterogeneous platforms from Khronos
  - Open standard
  - Modern C++
  - Commercial support from Intel with oneAPI/DPC++ and Codeplay
  - Open-source support growing to support wider set of platforms
- One possible option for programming CPUs, GPUs, etc in a performance portable way
Performance Portability of SYCL

- Paper at IWOCL explored performance on Intel CPUs and GPUs from Intel, AMD and NVIDIA.
- Comparisons with OpenCL, OpenMP, CUDA and HIP
- Very promising results so far, but more work to do in the HPC ecosystem
- Intel’s OpenCL runtime on CPUs has known issues which hopefully will improve as part of oneAPI

https://doi.org/10.1145/3388333.3388643
Performance Portability of SYCL

• Early work running SYCL on Arm
  • First results on ThunderX2 using hipSYCL on top of OpenMP
  • Performance close to native OpenMP for BabelStream
  • Known limitations of backend hipCPU implementation limit performance on all CPU platforms (both Intel and Arm) for more involved benchmarks
  • Currently exploring other avenues for SYCL on CPUs (Intel, AMD and Arm)

• SYCL’s future is looking bright:
  • Early view of SYCL-2020 shows lots of new HPC-friendly features
    • https://www.iwocl.org/iwocl-2020/conference-program/#panel
  • Support for NVIDIA GPUs added to open-source version of DPC++
  • Critical part of Argonne National Laboratory path to Exascale with Aurora
  • Robust support from/for Arm and AMD the next step

http://uob-hpc.github.io
IWOCL 2020
SYCLcon

The 8th International Workshop on OpenCL and the SYCL Developer Conference

Register for free and see the full programme online. Live panel with the OpenCL and SYCL standards developers on Tuesday April 28th from 4pm BST. Free SYCL tutorials on Monday April 27th and Wednesday April 29th:

www.iwocl.org

Thanks to our sponsors
SYCL v1.2.1 Specification
Click here to read or download the full Khronos® specification for SYCL™ 1.2.1 in PDF format.

Browse Implementations
Click here to find out where to get all the available SYCL implementations from.

Conformance Test Suite
The test suite is open source and hosted on GitHub. Contributions from the community to the CTS are welcome.

SYCL Working Group
Visit the SYCL™ Khronos® working-group’s home page to learn more about the SYCL technology.
Which performance portable programming model should I use?

- Want codes to run well everywhere, so how should I write them and what should I write them in?
- Tried a number of approaches:
  - Clone the code to allow study of performance portability
    - Multiple versions of the code exist
  - Lightweight interfaces to allow specialisation
    - Put simple library abstractions into the code
    - Portability layers like Kokkos is a grandiose approach to this
  - Performance portable standard programming models
    - OpenMP and SYCL offer the best hope today, but ecosystem needs support

http://uob-hpc.github.io/2020/05/05/choosing-models.html
Lessons learned about achieving performance portability

1. **Use open (standard) parallel programming languages** supported by multiple vendors across multiple hardware platforms
   - E.g. OpenMP, SYCL, Kokkos, Raja, ...?

2. **Expose maximal parallelism** at all levels of the algorithm and application

3. **Avoid over-optimising** for any one platform
   - Optimise for at least two different platforms at once

4. **Multi-objective autotuning** can significantly improve performance
   - Autotune for more than one target at once
   - See: Exploiting auto-tuning to analyze and improve performance portability on many-core architectures, J.Price and S. McIntosh-Smith, P^3MA, ISC’17

http://uob-hpc.github.io
• High Performance in silico Virtual Drug Screening on Many-Core Processors
  S. McIntosh-Smith, J. Price, R.B. Sessions, A.A. Ibarra, IJHPCA 2014

• On the performance portability of structured grid codes on many-core computer architectures
  S.N. McIntosh-Smith, M. Boulton, D. Curran, & J.R. Price
  ISC, Leipzig, June 2014. DOI: 10.1007/978-3-319-07518-1_4

• Assessing the Performance Portability of Modern Parallel Programming Models using TeaLeaf
  Martineau, M., McIntosh-Smith, S. & Gaudin, W.
  Concurrency and Computation: Practice and Experience (Apr 2016)

• GPU-STREAM v2.0: Benchmarking the achievable memory bandwidth of many-core processors across diverse parallel programming models
  Deakin, T. J., Price, J., Martineau, M. J. & McIntosh-Smith, S. N.
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For more information

Bristol HPC group:  https://uob-hpc.github.io/

Build & run scripts:


Twitter:  @simonmcs